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09/944,426	08/30/2001	Vladislav Vashchenko	75292/13356	1844

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EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/944,426	VASHCHENKO, VLADISLAV	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 9* is/are pending in the application.

4a) Of the above claim(s) *1* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 2-4 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitation of "a gate formed in the n-well ..... to define a high voltage node on one side of the gate", as recited in claim 2, is unclear as to how a gate can define a node on one side of itself.

The claimed limitation of "a gate, formed in the n-well, as recited in claim 2, is unclear as to how a gate can be formed in the n-well, since the gate is formed above the substrate.

The claimed limitation of "said at least one diode", as recited in claim 3, is unclear as to which whether said diode is the same diode recited earlier, or a different diode.

The claimed limitation of "the alternative current path defines a lower resistance current path than the p-well", as recited in claim 4, is unclear as to how a current path can be lower than a p-well.

The claimed limitations of "forming at least one additional p+ region and multiple additional n+ regions inside the p-well of the structure to define multiple diodes each with a p-n junction in the p-well, each diode being formed between a p-type material

andan n-type material, wherein the p-type material is defined by the p-well having one of the additional p+ regions or the second p+ region, as diode contact, and wherein the n-type material is defined by one of the additional n+ regions", as recited in claim 9, are unclear as to whether the element “at least one additional p+ region” “additional n+ regions” are part of or the same elements as the “additional p+ region” and “additional n+ region”, respectively, recited in independent claim 2, or different elements. It is further unclear whether the elements “diode” and “p-n junction” are the same elements recited in independent claim 2, or different elements.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4 and 9, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (6,573,566) in view of Yu (5,361,185).

Regarding claim 2, Ker et al. teach in figure 8B and related text a method of increasing the holding voltage of an LVTSCR structure that includes an n-well 208 and a p-well 206 formed in a substrate 200, a gate, a first n+ region 214 and a first p+ region 212 formed in the n-well to define a high voltage node on one side of the gate,

the method comprising:

forming an additional n+ region 220 inside the p-well of the structure to define a diode with a p-n junction between the additional n+ region and the p-well with the second p+ region forming a contact to the diode, and

the p-n junction being forward biased during normal operation by having said additional n+ region of the p-n junction located further from the high voltage node than the second p+ region.

Regarding claims 3-4, Ker et al. teach in figure 8B and related text a method of increasing the holding voltage of an LVTSCR structure having an anode in an n-well and a cathode in a p- well, comprising

forming at least one additional n+ region 220 and at least one additional p+ region 222 in the p-well to define at least one forward biased diode under normal operation in the p-well, thereby providing an alternative current path from anode to cathode through said at least one diode,

wherein the alternative current path defines a lower resistance current path than the p-well.

Ker et al. do not teach in the embodiment of figure 8B and a second n+ region and a second p+ region formed in the p-well to define a low voltage node on the other side of the gate.

Ker et al. teach in figure 10B a diode 324 connected to the cathode of SCR G2.

Yu teaches in figure 4 and related text a diode comprising an n+ region 50 and a p+ region 56 formed in a p substrate 24.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a diode comprising an n+ region and a p+ region in the p-well in Ker et al.'s device in order to provide better protection to the device, to reduce the size of the device by forming both diodes in the same well, and to simplify the processing steps of making the device.

Regarding claim 9 Yu teaches in figure 4 and related text forming at least one additional p+ region and multiple additional n+ regions inside the p-well of the structure to define multiple diodes each with a p-n junction in the p-well, each diode being formed between a p-type material andan n-type material, wherein the p-type material is defined by the p-well having one of the additional p+ regions or the second p+ region, as diode contact, and wherein the n-type material is defined by one of the additional n+ regions.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form forming at least one additional p+ region and multiple additional n+ regions inside the p-well of the structure to define multiple diodes each with a p-n junction in the p-well, each diode being formed between a p-type material andan n-type material, wherein the p-type material is defined by the p-well having one of the additional p+ regions or the second p+ region, as diode contact, and wherein the n-type material is defined by one of the additional n+ regions, in Ker et al.'s device in order to provide better protection to the device.

Response to Arguments

Applicant argues that the claimed limitation of "a gate formed in the n-well ..... to define a high voltage node on one side of the gate", as recited in claim 2, is clear, because "claim 2 does not define the gate as forming a node. Instead, claim 2 states that there is a high voltage node on one side of the gate and a low voltage node on the other side of the gate". Applicant further argues that "claim 2 does not state that there is a gate in the n-well. It simply states that the LVTSCR includes a gate. There is a comma after the word "gate". It is the first n+ region and the first p+ region that are formed in the n-well according to claim 2".

Although there is a comma after the word "gate", the passage "a method of increasing the holding voltage of an LVTSCR structure that includes an n-well and a p-well formed in a substrate, a gate, a first n+ region and a first p+ region formed in the n-well to define a high voltage node on one side of the gate", means that the term "gate" must be associated with the phrase "a first n+ region and a first p+ region formed in the n-well to define a high voltage node on one side of the gate" and not with the phrase "a method of increasing the holding voltage of an LVTSCR structure that includes an n-well and a p-well formed in a substrate". If the term "gate" is associated with the phrase "a method of increasing the holding voltage of an LVTSCR structure that includes an n-well and a p-well formed in a substrate" to recite "a method of increasing the holding voltage of an LVTSCR structure that includes an n-well and a p-well formed in a substrate, a gate", as argued by applicant, then the claim is unclear as to the structural relationship between the element "gate" and the LVTSCR structure.

Applicant argues that the phrase "said at least one diode", as recited in claim 3, is clear, because "The use of the word "said" is standard claim language terminology to explicitly refer to the previously cited element. Since there is no other diode or set of diodes it has to refer to the earlier mentioned diode or set of diodes".

Claim 3 recites element A by the name "at least one forward biased diode". The claim then recites element B by the name "at least one diode". Element A has different name from element B. Since applicant cannot call one element by two different names, then element A must be different from element B. However, the claim recites "said at least one diode". Therefore, it is unclear as to which diode applicant refers by reciting "said at least one diode".

Applicant argues that "Regarding claim 4 the Office action states that it is unclear how a current path can be lower than a p-well. It is respectfully pointed out that the current path is not lower. Instead the resistance of the current path is lower since it includes the diodes".

Claim 4 recites the limitation of "the alternative current path defines a lower resistance current path than the p-well". The phrase "a lower resistance current path **than the p-well**" mean that the current path is lower **than a p-well**. In other words, something is "**than the p-well**" and it is unclear what is "**than the p-well**".

Applicant argues that figure 8 of Ker provides second n+ and p+ regions 220, 222 in the p-well, and "Ker does not teach or suggest providing an additional n+ region

in the p-well, over and above the second n+ and second p+ regions of the standard LVTSCR".

The examiner agrees that figure 8 of Ker does not provide an additional n+ region in the p-well, over and above the second n+ and second p+ regions of the standard LVTSCR. However, figure 10B of Ker teaches a diode 324 connected to the cathode of SCR G2. Therefore, forming diode 324 in the device of the embodiment of figure 8B of Ker et al. will provide "an additional n+ region in the p-well, over and above the second n+ and second p+ regions of the standard LVTSCR".

Applicant argues that an artisan will not be motivated to add additional diodes in the p-well of Ker et al., because "the external diodes shown in Ker are provided not between anode and cathode of the SCR device but between cathode and Vss". Applicant further argues that "It cannot therefore be said that it would be obvious to provide internal diodes in Ker because that would cause the opposite effect to what Ker is trying to achieve".

The examiner does not suggested to form Ker et al.'s external diode because the anode and cathode of Ker et al.'s device. The examiner merely suggests forming the external diode in the p-well. Thus, merely forming the external diode in the p-well will not cause the opposite effect to what Ker is trying to achieve.

Note that the broad recitation of the claims does not require that all the diodes must be formed between the anode and the cathode of the LVTSCR structure. **The examiner agrees that a claim recitation wherein the plurality of the internal diodes**

is formed between the cathode and the anode of the LVTSCR structure, will overcome the rejection over Ker et al. Applicant is invited to contact the examiner to discuss an amendment which will overcome the rejection over Ker et al.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
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